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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,795	02/20/2004	Yasuyuki Arai	0756-7256	5184

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,795	ARAI ET AL.	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-14 and 24-27* is/are allowed.

6)☒ Claim(s) *1-9,11 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/25/2008 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. No. 2003/0032210 to Takayama et al (Takayama) in view of U.S. Pub. No. 2002/0146893 to Shimoda et al. (Shimoda).

Regarding claim 1, Takayama discloses a semiconductor device comprising a thin film integrated circuit device (Figures 9A-9D), where the thin film integrated circuit comprises: a substrate (412); an adhesive (411) over the substrate; a metal oxide (402; paragraph [0190] lines 1-3, paragraph [0242] lines 17-18, paragraph [0246] line 4) over the adhesive; an insulating film (403; paragraph [0191] lines 1, paragraph [0242] lines 19-20) over the metal oxide; a

first and second semiconductor film (104-108 in Figure 6A) on and in contact with the insulating film (104-108 on and in contact with insulating film 103), and a transistor comprising the second semiconductor film (104-108 in Figure 6A), a gate insulating film (118 in Figure 6B), and a gate electrode (Figure 6C elements 126-130), wherein the second semiconductor film (104-108 in Figure 6A)is formed on and in contact with the insulating film (104-108 on and in contact with insulating film 103).

Takayama also discloses the ability for a device to be combined with a memory element (paragraph [0301]), however Takayama fails to explicitly disclose a memory comprising a first semiconductor film. Shimoda discloses a first semiconductor film used as a memory (within thin film layer 4, paragraph [0119] line 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takayama to have the first semiconductor film as a memory like in Shimoda in order to provide an integrated circuit capable of storing data.

Regarding claims 4 and 5, Takayama discloses a semiconductor device according to claim 1, where the first semiconductor film functions as an active region and as a channel region (paragraph [0217] and [0221])

Regarding claim 6, Takayama discloses an IC label comrpsing a thin film integrated circuit, where the thin film integrated circuit comprises: a substrate (412); an adhesive (411) over the substrate; a metal oxide (402; paragraph [0190] lines 1-3, paragraph [0242] lines 17-18, paragraph [0246] line 4) over the adhesive; an insulating film (403; paragraph [0191] lines 1, paragraph [0242]

lines 19-20) over the metal oxide; a first and second semiconductor film (104-108 in Figure 6A) on and in contact with the insulating film (104-108 on and in contact with insulating film 103), and a transistor comprising the second semiconductor film (104-108 in Figure 6A), a gate insulating film (118 in Figure 6B), and a gate electrode (Figure 6C elements 126-130), wherein the second semiconductor film (104-108 in Figure 6A)is formed on and in contact with the insulating film (104-108 on and in contact with insulating film 103).

Takayama also discloses the ability for a device to be combined with a memory element (paragraph [0301]), however Takayama fails to explicitly disclose a memory comprising a first semiconductor film. Shimoda discloses a first semiconductor film used as a memory (within thin film layer 4, paragraph [0119]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takayama to have the first semiconductor film as a memory like in Shimoda in order to provide an integrated circuit capable of storing data.

Regarding claim 15, Takayama discloses a container comrpsing a thin film integrated circuit, where the thin film integrated circuit comprises: a substrate (412); an adhesive (411) over the substrate; a metal oxide (402; paragraph [0190] lines 1-3, paragraph [0242] lines 17-18, paragraph [0246] line 4) over the adhesive; an insulating film (403; paragraph [0191] lines 1, paragraph [0242] lines 19-20) over the metal oxide; a first and second semiconductor film (104-108 in Figure 6A) on and in contact with the insulating film (104-108 on and in contact with insulating film 103), and a transistor comprising the second semiconductor

film (104-108 in Figure 6A), a gate insulating film (118 in Figure 6B), and a gate electrode (Figure 6C elements 126-130), wherein the second semiconductor film (104-108 in Figure 6A)is formed on and in contact with the insulating film (104-108 on and in contact with insulating film 103).

Takayama also discloses the ability for a device to be combined with a memory element (paragraph [0301]), however Takayama fails to explicitly disclose a memory comprising a first semiconductor film. Shimoda discloses a first semiconductor film used as a memory (within thin film layer 4, paragraph [0119]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takayama to have the first semiconductor film as a memory like in Shimoda in order to provide an integrated circuit capable of storing data.

Regarding claim 16, Takayama discloses a container according to claim 15 as above. Takayama discloses where the thin film integrated circuit is covered by a label (407).

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. No. 2003/0032210 to Takayama et al (Takayama) in view of U.S. Pub. No. 2002/0146893 to Shimoda et al. (Shimoda) and U.S. Pat. No. 6,703,267 to Tanabe et al (Tanabe).

Regarding claims 2-3, Takayama discloses a semiconductor device according to claim 1.

Takayama fails to disclose:

- the metal oxide as an oxide of an element selected from the group consisting of W, Ti, Ta, Mo, Nd, Ni, Co, Zr, Zn, Ru, Rh, Pd, Os, and Ir; an alloy containing the metal as a main component; or a chemical compound thereof or WO_2 or WO_3.

Tanabe teaches:

- a thin film integrated circuit device (Figure 11c) with the metal oxide as WO_2 or WO_3 (Column 3 line 24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takayama to have the metal oxide as WO_2 or WO_3 as in Tanabe et al. in order to form a good interface between the metal oxide and the insulating layer.

Claims 7-8 and 18-19 are rejected under 35 U.S.C. 103(a) as being anticipated by U.S. Pub. No. 2003/0032210 to Takayama in view of U.S. Pub. No. 2002/0146893 to Shimoda et al. (Shimoda) and U.S. Pat. No 6,885,032 to Forbes et al. (Forbes).

Regarding claims 7-8 and 18-19, Takayama discloses an IC label and a container with a thin film integrated circuit as above in claims 6 and 15.

Takayama fails to disclose:

- the IC label as contactless
- where the surface can be printed with a character, a letter, text, a symbol, or a diagram.

- where the thin film integrated circuit is held between a first label and a second label film and the second label is affixed to the thin film integrated circuit with an adhesive agent
- and the metal oxide adhered to the container

Forbes teaches:

- an IC label (Figure 2c element 16') as a contactless type (column 2 lines 39-47)
- a surface of the IC label (Figure 1 element 16) can be printed with a character, a letter, text, a symbol, or a diagram (Figure 1 element 14 and column 2 line 9-12).
- the thin film integrated circuit (Figure 2a element 20) is held between a first label (Figure 2b elements 22 and 24) and a second label film (Figure 5 element 32), and the second label is affixed to the thin film integrated circuit with an adhesive agent (Figure 5 element 36).
- and the metal oxide adhered to the container (Figure 1 and column 5 lines 11-19).

It would have been obvious to one of ordinary skill in the art at the time the invention was made in order to allow the integrated circuit to be used for applications such as RFID tags.

Claims 9, 11, 20-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. No. 2003/0032210 to Takayama in view of

U.S. Pub. No. 2002/0146893 to Shimoda et al. (Shimoda) and U.S. Pat. No 6,885,032 to Forbes et al. and U.S. Pub. No. 2004/0256644 to Kugler et al.

Regarding claims 9 and 11, Takayama discloses an IC label comprising a thin film integrated circuit where the thin film integrated circuit comprises a substrate (412), an adhesive (411) over the substrate; a metal oxide (402; paragraph [0190] lines 1-3, paragraph [0242] lines 17-18, paragraph [0246] line 4) over the adhesive; an insulating film (403; paragraph [0191] lines 1, paragraph [0242] lines 19-20) over the metal oxide, a semiconductor film (104-108 in Figure 6A), a gate insulating film (118 in Figure 6B) and a gate electrode (Figure 6C elements 126-130), which are provided over the insulating film. Takayama also discloses use of the label with an antenna (2906 in Figure 19A and 3006 in Figure 19B).

Takayama fails to disclose:

- the IC label comprising a contactless thin film integrated circuit.
- the antenna in a same layer as the gate electrode.
- the antenna with the same material as the gate electrode.
- the antenna comprising a conductive paste.

Forbes teaches:

- an IC label (Figure 2 element 16') comprising a contactless thin film integrated circuit (column 2 lines 39-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takayama to include a contactless thin film

integrated circuit as in Forbes in order to allow the integrated circuit to be used for applications such as RFID tags.

Kugler et al. teaches:

- an antenna in the same layer as the gate electrode (page 7 paragraph 75 lines 6-7).
- the antenna formed from the same material as the gate electrode (page 2 paragraph 22 lines 5-8).
- the antenna comprising a conductive paste (page 7 paragraph 76 lines 3-5).
- the gate electrode and the antenna are formed on and in contact with the gate insulating film (both the antenna and gate electrode are in the same layer (paragraph [0022]) and a common plane (paragraph [0023])).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add an antenna in the same layer as the gate electrode make the antenna with the same material as the gate electrode or a conductive paste to Takayama in order to provide an identification device with an active antenna that can be deposited on a substrate with conventional printing methods.

Regarding claims 20 and 23, Takayama discloses a container comprising a thin film integrated circuit where the thin film integrated circuit comprises a substrate (412), an adhesive (411) over the substrate; a metal oxide (402; paragraph [0190] lines 1-3, paragraph [0242] lines 17-18, paragraph [0246] line 4) over the adhesive; an insulating film (403; paragraph [0191] lines 1,

paragraph [0242] lines 19-20) over the metal oxide, a semiconductor film (104-108 in Figure 6A), a gate insulating film (118 in Figure 6B) and a gate electrode (Figure 6C elements 126-130), which are provided over the insulating film. Takayama also discloses use of the container with an antenna (2906 in Figure 19A and 3006 in Figure 19B).

Takayama fails to disclose:

- the container comprising a contactless thin film integrated circuit.
- an antenna formed from the same material as the gate electrode
- the thin film integrated circuit held between a first label and a second label and the second label is affixed to the thin film integrated circuit with an adhesive agent.

Forbes teaches:

- an IC label (Figure 2c element 16') as a contactless type (column 2 lines 39-47)
- the thin film integrated circuit (Figure 2a element 20) held between a first label (Figure 2b elements 22 and 24) and a second label (Figure 5 element 32), and the second label is affixed to the thin film integrated circuit with an adhesive agent (Figure 5 element 36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takayama to have a container comprising the contactless thin film integrated circuit adhered to the container as in Forbes in order to attach the IC to a products such as cell phones or RFID tags.

Kugler et al. teaches:

- the antenna formed from the same material as the gate electrode (page 2 paragraph 22 lines 5-8).
- the gate electrode and the antenna are formed on and in contact with the gate insulating film (both the antenna and gate electrode are in the same layer (paragraph [0022]) and a common plane (paragraph [0023])).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add an antenna in the same layer as the gate electrode to further modify Takayama in order to provide an identification device with an active antenna that can be deposited on a substrate with conventional printing methods.

Regarding claim 21, Takayama as modified discloses a container according to claim 20 as above. Takayama discloses where the thin film integrated circuit is covered by a label (407).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. No. 2003/0032210 to Takayama in view of U.S. Pub. No. 2002/0146893 to Shimoda et al. (Shimoda) and U.S. Pub. No. 2002/0027247 to Arao et al.

Regarding claim 17, Takayama discloses a container according to claim 16 as outlined above.

Takayama fails to disclose:

- the protective film having a DLC or CN film

Arao et al. teaches:

- a protective film of DLC (Figure 10B element 704) provided on a thin film integrate circuit.

It would have been obvious to one of ordinary skill in the art at the time the invention was made use the DLC film of Arao et al. as the protection layer in Takayama in order to prevent the invasion of oxygen as well as water and also to mechanically protect the thin film integrated circuit.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. No. 2003/0032210 to Takayama in view of U.S. Pub. No. 2002/0146893 to Shimoda et al. (Shimoda) and U.S. Pat. No 6,885,032 to Forbes et al. and U.S. Pub. No. 2004/0256644 to Kugler et al in further view of U.S. Pub. No. 2002/0027247 to Arao et al (Arao).

Regarding claim 22, Takayama as modified teaches a container according to claim 21 as outlined above.

Takayama fails to disclose:

- the protective film having a DLC or CN film

Arao et al. teaches:

- a protective film of DLC (Figure 10B element 704) provided on a thin film integrate circuit.

It would have been obvious to one of ordinary skill in the art at the time the invention was made use the DLC film of Arao et al. as the protection layer in

Takayama in order to prevent the invasion of oxygen as well as water and also to mechanically protect the thin film integrated circuit.

Allowable Subject Matter

Claims 12-14 and 24-27 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claims 12 and 24, the prior art fails to anticipate or render obvious the thin film integrated circuit with the limitations including an antenna provided on the interlayer insulating film.

Response to Arguments

Applicant's arguments filed 04/25/2008 have been fully considered but they are not persuasive.

Applicant argues (Remarks page 10 paragraph 2) that it "appears that Shimoda merey discloses a thin film transistor using silicond but not a memory comprising a semiconductor film." Examiner disagrees. Shimoda's disclosure is directed to thin films of semiconductor layers, as evident by for example paragraph [0003] disclosing use of materials such as silicon. Paragraph [0119] recites "transferred layer 4 be a thin film, and particularly a function thin film or thin film device" (lines 4-6). One of ordinary skill in the art would understand these thin films to include semiconductor thin films. Paragraph [0119] further states that an example of the **functional thin film includes "memories" (line**

11). One of ordinary skill in the art would understand the language of Shimoda, which also recites the the examples are not limited, to encompass thin films of semiconductor layers in a memory device.

Applicant argues (Remarks page 10 paragraph 2) that prior art fails to disclose the first and second semiconductor films formed on and in contact with an insulating film. Examiner disagrees, semiconductor films 104-108 are formed on and in contact with insulating film 103 as shown in Fig 6A.

Applicant argues (Remarks page 10 paragraph 3) that the examiner has not provided a teaching suggesting or motivation to combine references. The examiner disagrees. One would have been motivated to do so at the time of the invention to provide RFID capabilities as mentioned in Kugler (paragraph [0001]) while also using conventional manufacturing methods.

Applicant argues (Remarks page 10 paragraph 5 – page 11 paragraph 3) that the prior art do not teach the gate electrode formed over the gate insulation film. Kugler discloses the antenna in the same layer as the gate electrode and Takayama discloses the gate electrode above the gate insulation film, thus Kugler's antenna would also be above the gate insulation film.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is (571)272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A. M./
Examiner, Art Unit 2811

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811